

CLAIMS

What is claimed is:

1. A method of generating synthesis scripts to synthesize integrated circuit (IC) designs from a generic netlist description into gate-level description, said method comprising the steps of:

- 5 identifying hardware elements in the generic netlist;
determining key pins for each of said identified hardware elements;
extracting design structure and hierarchy from the Generic netlist;
generating script to cause a logic synthesis tool to apply bottom-up synthesis to modules and sub-modules of the IC design;
generating script to cause a logic synthesis tool to apply top-down
10 characterization to modules and sub-modules of the IC design; and
generating script to cause a logic synthesis tool to repeat said bottom-up and said top-down applications until constraints are satisfied.

2. A method according to claim 1 wherein said step of extracting design structure allows for a multilevel structuring of modules of the IC design.

3. A method according to claim 1 further comprising the step of generating script to cause a logic synthesis tool to apply initial mapping to the IC design.

4. A method according to claim 1 wherein the logic synthesis tool is Synopsys Design Compiler.

5. A method according to claim 1 further comprising the step of rearranging design hierarchy by changing the design.

6. A method according to claim 1 further comprising the step of generating

~~SECRET~~

\triangleleft a'

- 1993

30454-122 (P-3605)

means for determining key pins for each of said identified hardware elements;
means for extracting critical design structure and hierarchy from the generic
netlist;
means for applying bottom-up synthesis to modules and sub-modules of the IC
5 design;
means for applying top-down characterization to modules and sub-modules of
the IC design;
means for repeating said bottom-up and said top-down applications until
constraints are satisfied; and
10 means for creating design compile scripts to synthesize modules and sub-
modules and the IC design having said satisfied constraints.

11. A computer storage medium containing instructions for generating
synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description
into gate-level description, said instructions comprising the steps of:

identifying hardware elements in the generic netlist;
5 determining key pins for each of said identified hardware elements;
extracting critical design structure and hierarchy from the generic netlist;
applying bottom-up synthesis to modules and sub-modules of the IC design;
applying top-down characterization to modules and sub-modules of the IC
design;

10 repeating said bottom-up and said top-down applications until constraints are
satisfied; and

creating design compile scripts to synthesize modules and sub-modules and the
IC design having said satisfied constraints.

12. A computer storage medium of claim 11 wherein said computer storage
medium is selected from a group consisting of magnetic device, optical device,
magneto-optical device, floppy diskette, CD-ROM, magnetic tape, computer hard
drive, and memory card.

09026700-022098

sub
a1

30454-122 (P-3605)

13. A process for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, said process comprising the steps of:

- identifying hardware elements in the generic netlist;
- 5 determining key pins for each of said identified hardware elements;
- extracting critical design structure and hierarchy from the generic netlist;
- applying bottom-up synthesis to modules and sub-modules of the IC design;
- applying top-down characterization to modules and sub-modules of the IC design;
- 10 repeating said bottom-up and said top-down applications until constraints are satisfied; and
- creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.

14. A computer system for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, said system comprising:

- means for determining key pins for each of said identified hardware elements;
- 5 means for extracting critical design structure and hierarchy from the generic netlist;
- means for applying bottom-up synthesis to modules and sub-modules of the IC design;
- means for applying top-down characterization to modules and sub-modules of
- 10 the IC design;
- means for repeating said bottom-up and said top-down applications until constraints are satisfied; and
- means for creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.